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Scala3-15/17CRV

CPU : Sandy / IVY Bridge PGA
Chip Set : Intel Panther Point
GFX : NVIDIA N13M-GE1/GS
Remarks : Chief River Platform

Model Name : Scala3-15/17CRV
PBA Name : MAIN_Dual
PCB Code : BA41-01976A
BA41-01977A
BA41-01978A
BA41-01979A
Dev. Step : PVR
Revision : 1.0
T.R. Date : 2012.02.27

Design	CHECK	APPROVAL
<i>Sen Li</i>	<i>RJ Zheng</i>	<i>BL LEE</i>

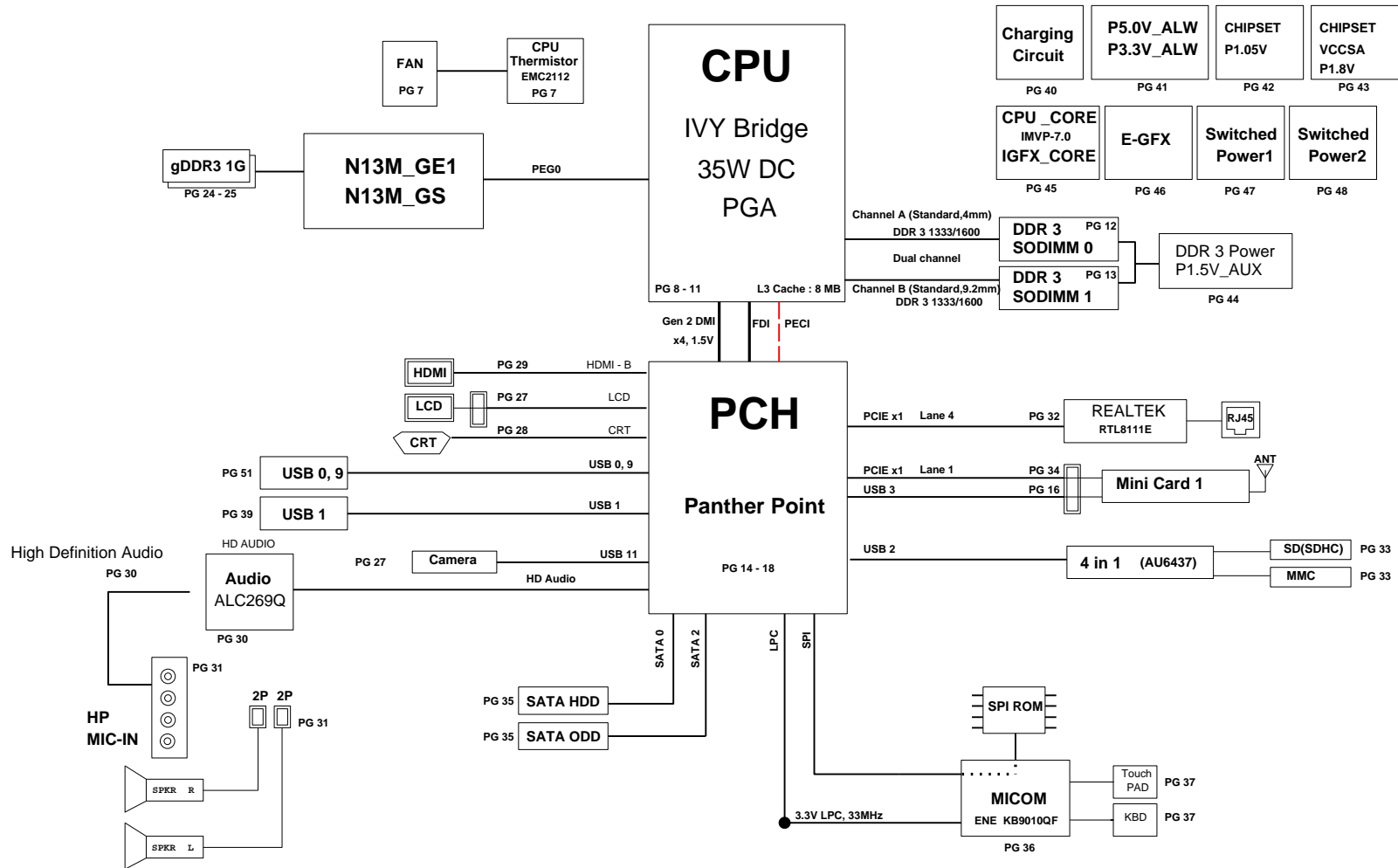
■ Owner : SEC Mobile R & D Signature : X

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DRAW	Sen Li	DATE	02/27/2012	TITLE	Scala3-15/17CRV	SAMSUNG ELECTRONICS PART NO. BA41-01976A
CHECK	RJ Zheng	DEV. STEP	PR		MAIN	
APPROVAL	BL LEE	REV	REV 1.0		COVER	
MODULE CODE		LAST EDIT	February 24, 2012 19:05:49 PM	PAGE	1 OF 51	

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BLOCK DIAGRAM



DRAW	Sen Li	DATE	02/27/2012	TITLE	Scala3-15/17CRV	SAMSUNG ELECTRONICS
CHECK	RJ Zheng	DEV. STEP	PR	MAIN		
APPROVAL	BL LEE	REV	REV 1.0	BLOCK DIAGRAM	PART NO. BA41-01976A	
MODULE CODE	undefined	LAST EDIT		February 24, 2012 19:05:49 PM	PAGE	2 OF 51

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BOARD INFORMATION

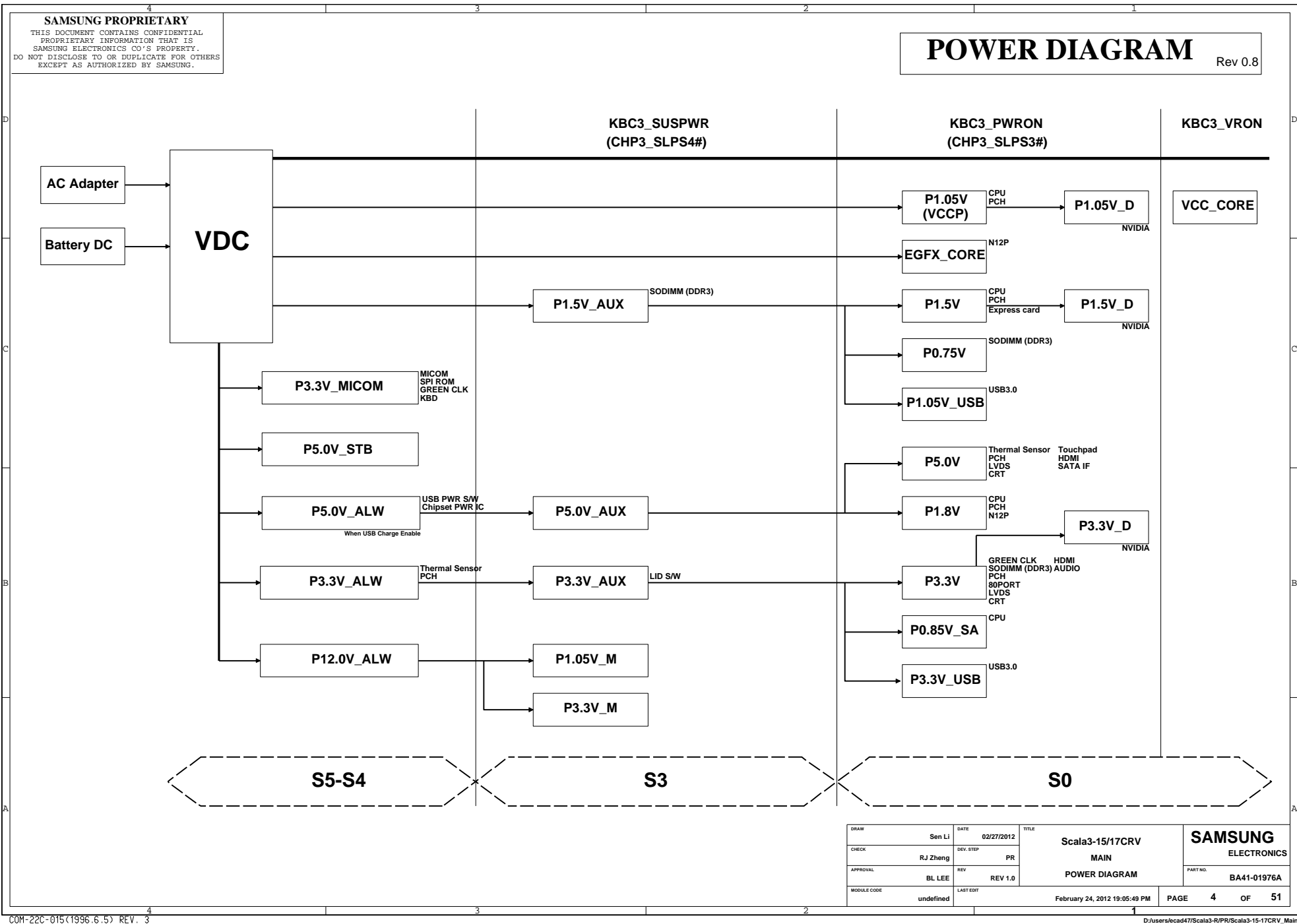
SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

SATA PORT Assign	
PORT #	ASSIGNED TO
0	HDD
1	NC
2	ODD
3	NC
4	NC
5	NC

Crystal / Oscillator			
TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	HM75	Real Time Clock
Crystal	25MHz	LAN	Intel LAN
Crystal	25MHz	GREENCLK	GREENCLK
Crystal	25MHz	HM75	INTEL
Crystal	27MHz	N13M-GE1/GS	NVIDIA

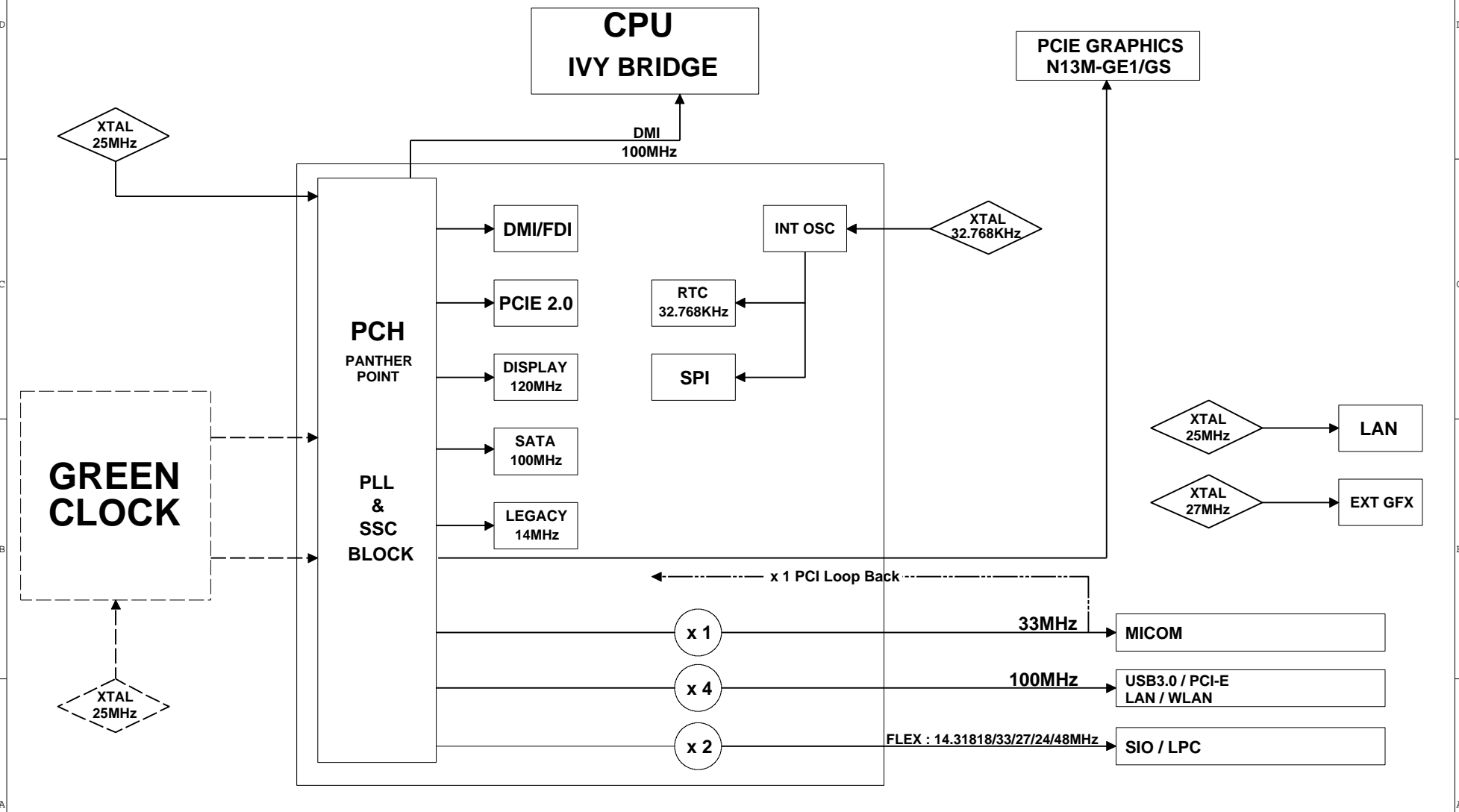
LCD Pannel Detect (TBD)		
Devices	Resolution	PANNEL_DETECT_0

DRAW		Sen Li	DATE	02/27/2012	Scala3-15/17CRV MAIN BOARD INFO	SAMSUNG ELECTRONICS
CHECK		RJ Zheng	DEV. STEP	PR		
APPROVAL		BL LEE	REV	REV 1.0		
MODULE CODE		undefined	LAST EDIT			
					February 24, 2012 19:05:49 PM	PAGE 3 OF 51



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CLOCK DISTRIBUTION Rev. 0.8

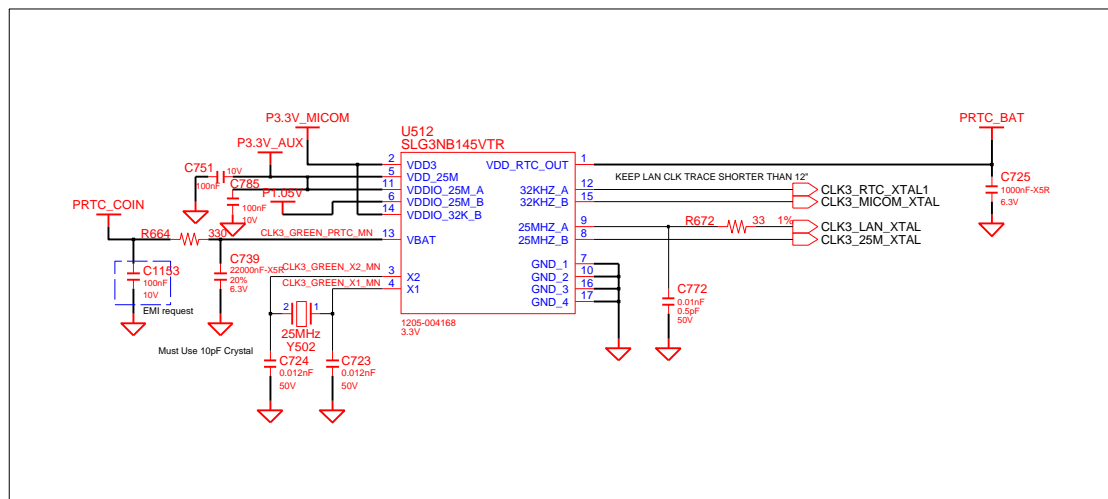


DRAW	Sen Li	DATE	02/27/2012	TITLE	Scala3-15/17CRV	SAMSUNG ELECTRONICS PART NO. BA41-01976A
CHECK	RJ Zheng	DEV. STEP	PR		MAIN	
APPROVAL	BL LEE	REV	REV 1.0		CLOCK DIAGRAM	
MODULE CODE	undefined	LAST EDIT	February 24, 2012 19:05:49 PM	PAGE	5 OF 51	

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CLOCK DISTRIBUTOR



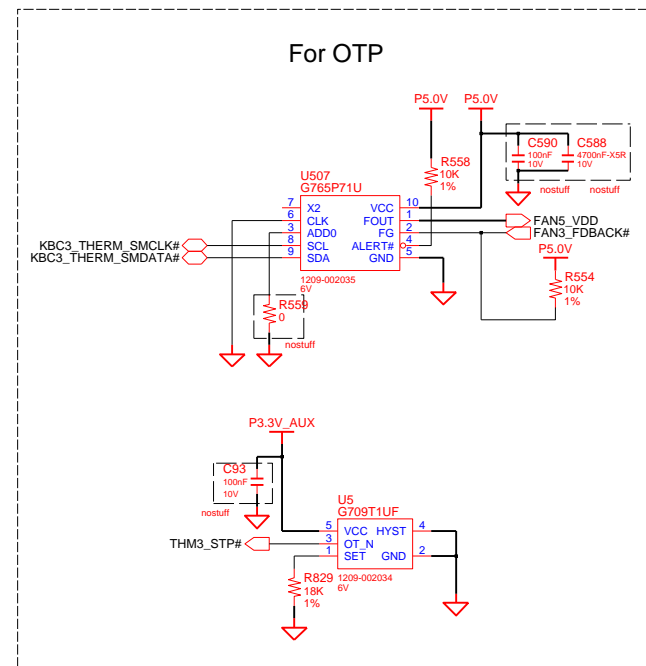
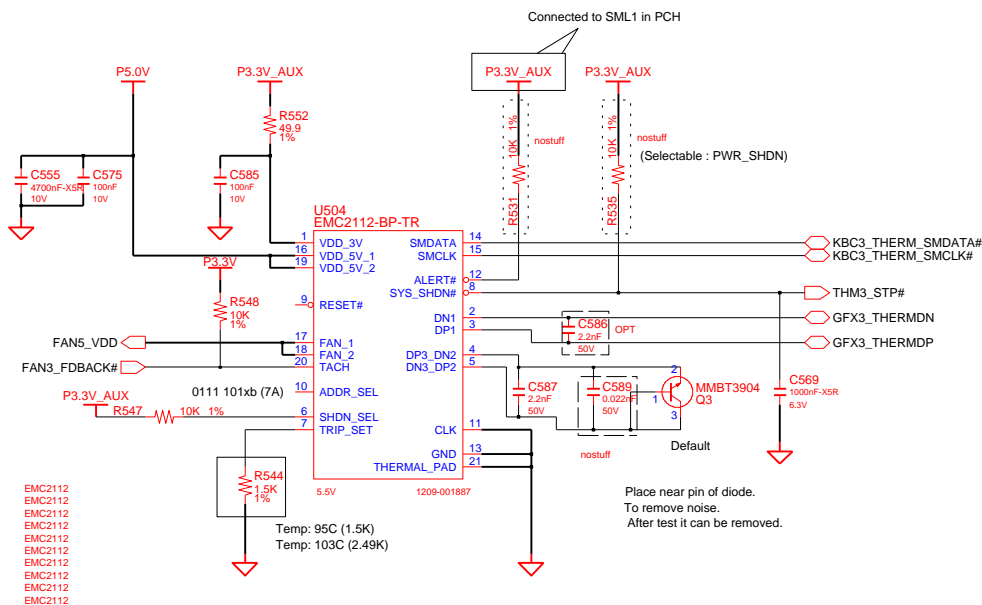
GREENCLK
GREENCLK
GREENCLK
GREENCLK
GREENCLK
GREENCLK
GREENCLK
GREENCLK
GREENCLK
GREENCLK

DRAW	Sen Li	DATE	02/27/2012	TITLE	Scala3-15/17CRV CLOCK CLOCK DISTRIBUTION	SAMSUNG ELECTRONICS
CHECK	RJ Zheng	DEV. STEP	PR			PART NO. BA41-01976A
APPROVAL	BL LEE	REV	REV 1.0			
MODULE CODE	undefined	LAST EDIT	February 24, 2012 19:05:49 PM	PAGE	6	OF 51

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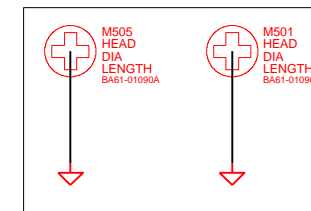
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THERMAL SENSOR & FAN CONTROL



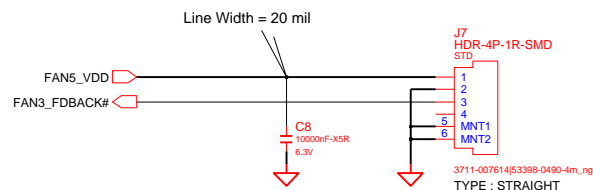
Temperature : 95.78c
confirmed by thermal charger
(2011.05.02)
 $R_{th}(\text{kohm}) = 0.0012T^{\circ} - 0.9308T + 96.147$

FAN PEM



ADDRESSSEL MODE	
0	0101 111xb
✓ HIGH Z	0111 101xb (7A)
1	0101 110xb

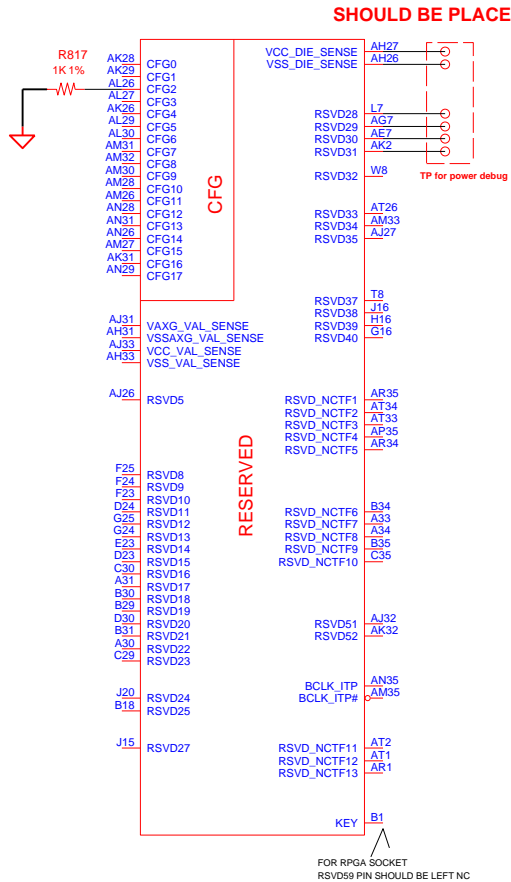
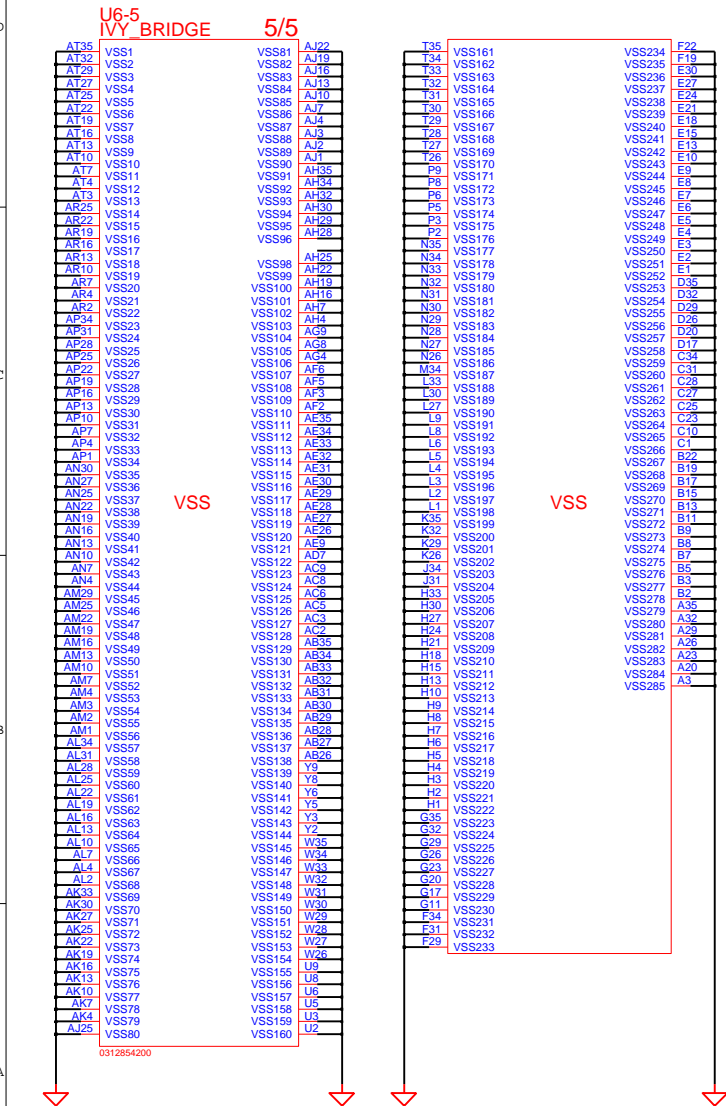
SHDN_SEL MODE	
0	INTEL TR MODE
✓ HIGH Z	AMD CPU/DIODE MODE
1	EXT.DIODE 2 MODE



DESIGN	Sen Li	DATE	02/27/2012	TITLE	Scala3-15/17CRV
CHECK	RJ Zheng	DEV. STEP	PR		THERMAL SENSOR
APPROVAL	BL LEE	REV	REV 1.0		THERMAL SENSOR EMC2112
MODULE CODE		LAST EDIT		February 24, 2012 19:05:49 PM	PAGE 7 OF 51

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PART NO.
BA41-01976A

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PEG STATIC LANE REVERSAL - CFG2 IS FOR THE 16X	
CFG2	1 : (DEFAULT) NORMAL OPERATION 0 : LANE REVERSED

PCIe PORT BIFURCATION STRAPS	
CFG[6:5]	11 : (DEFAULT) X16 - DEVICE 1 FUNCTIONS 1 AND 2 DISABLED 10 : X8, X8 - DEVICE 1 FUNCTION 1 ENABLED ; FUNCTION 2 DISABLED 01 : RESERVED - (DEVICE 1 FUNCTION 1 DISABLED ; FUNCTION 2 ENABLED) 00 : X8, X4, X4 - DEVICE 1 FUNCTIONS 1 AND 2 ENABLED

Display Port Presence	
CFG4	1 : Disabled - No DP device is connected to eDP 0 : Enabled - (DP device is connected to eDP)

PEG DEFER TRAINING	
CFG7	1 : (DEFAULT) PEG TRAIN IMMEDIATELY FOLLOWING XXRESETB DEASSERTION 0 : PEG WAIT FOR BIOS FOR TRAINING

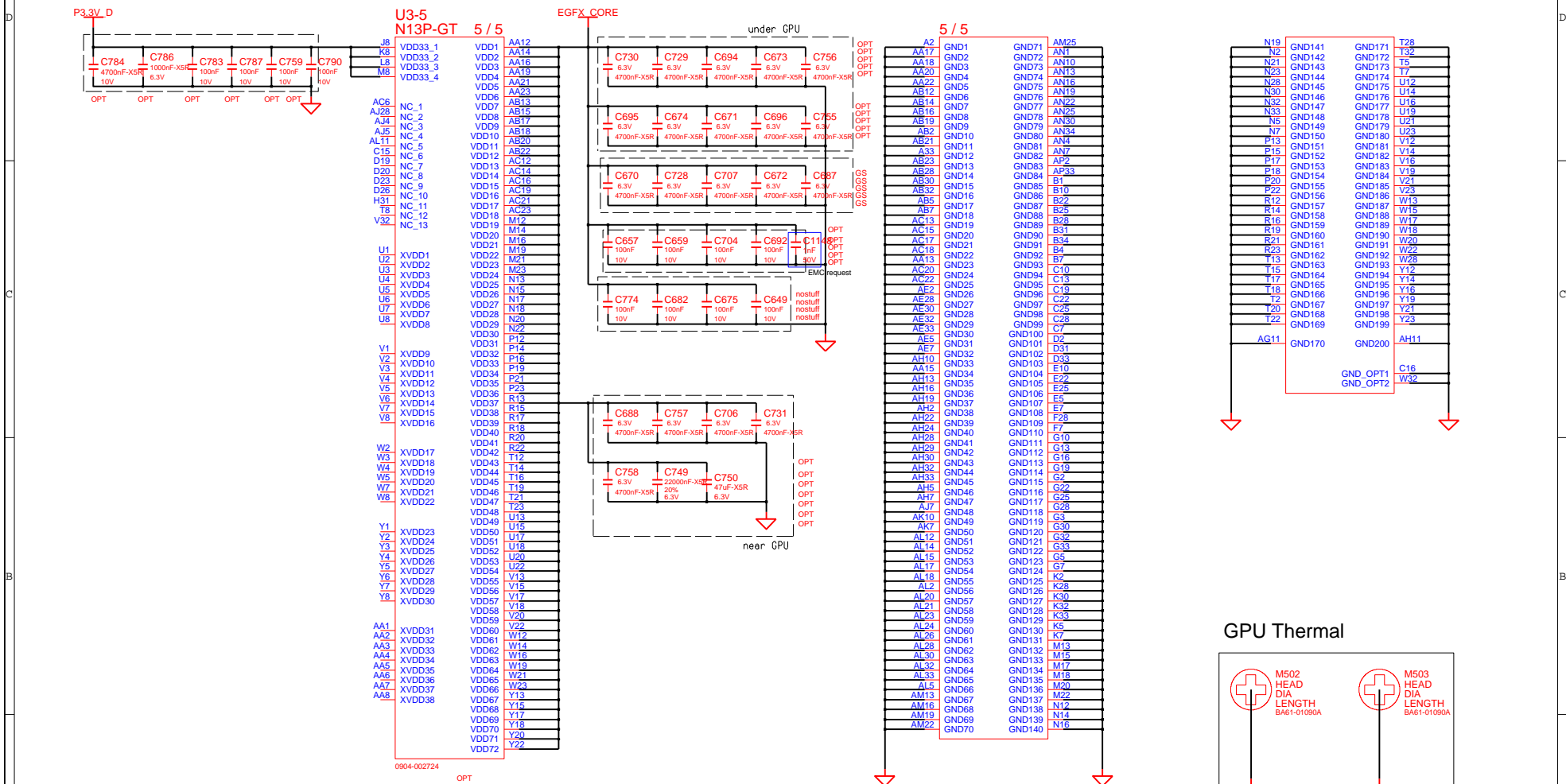
DESIGN	Sen Li	DATE	02/27/2012	TITLE	Scala3-15/17CRV	SAMSUNG ELECTRONICS PART NO. BA41-01976A
CHECK	RJ Zheng	DEV. STEP	PR		CPU	
APPROVAL	BL LEE	REV	REV 1.0		Sandy / IVY Bridge (4/4)	
MODULE CODE		LAST EDIT		February 24, 2012 19:05:49 PM	PAGE	11 OF 51

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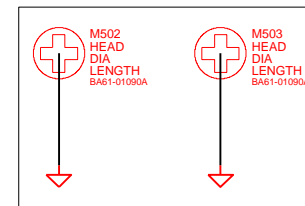


COM-22C-015(1996.6.5) REV. 3

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GPU Thermal



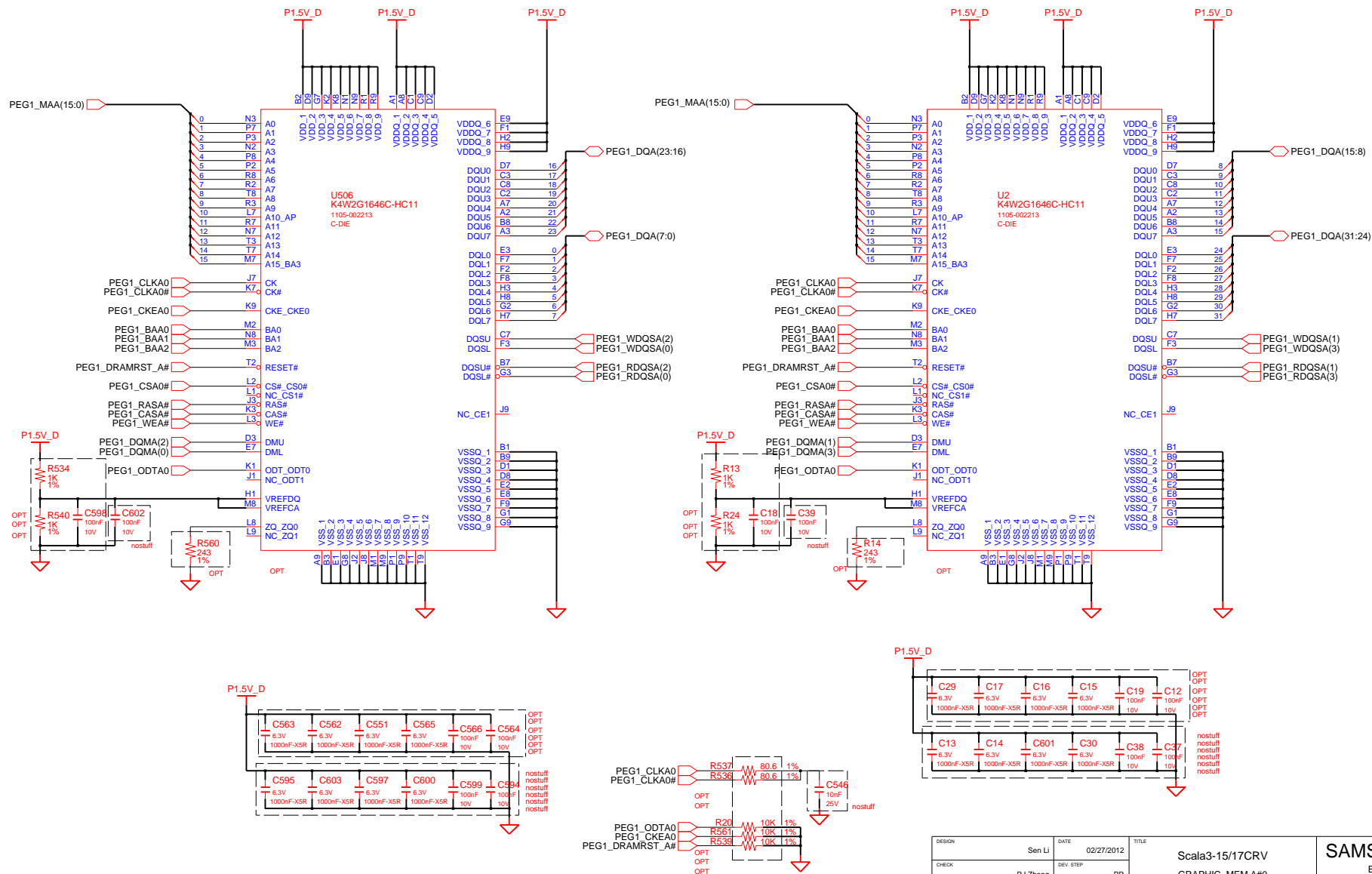
INT GFX and OPT GFX model need.

DESIGN	Sen Li	DATE	02/27/2012	TITLE	Scala3-15/17CRV	SAMSUNG
CHECK	RJ Zheng	DEV. STEP	PR		N13X_40NM(5/5)	ELECTRONICS
APPROVAL	BL LEE	REV	REV 1.0		N13X_40NM(5/5)	PART NO.
MODULE CODE		LAST EDIT				BA41-01976A
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A-Channel #0 (D-mode)



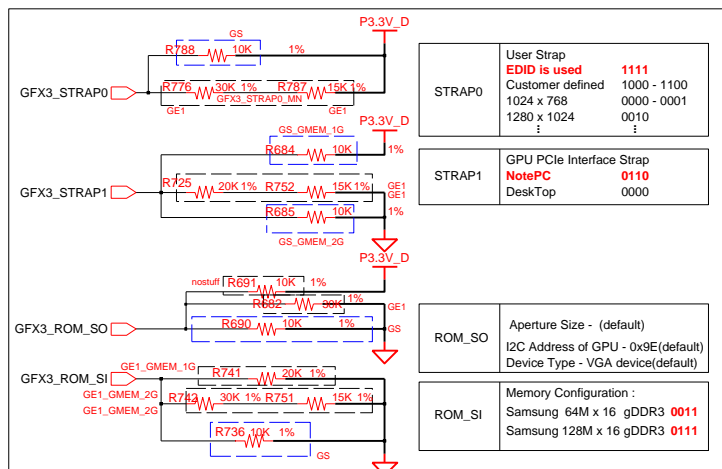
DESIGN	Sen Li	DATE	02/27/2012	TITLE	Scala3-15/17CRV	SAMSUNG ELECTRONICS
CHECK	RJ Zheng	DEV. STEP	PR		GRAPHIC_MEM A#0	
APPROVAL	BL LEE	REV	REV 1.0		GRAPHIC_MEM A#0	
MODULE CODE		LAST EDIT				
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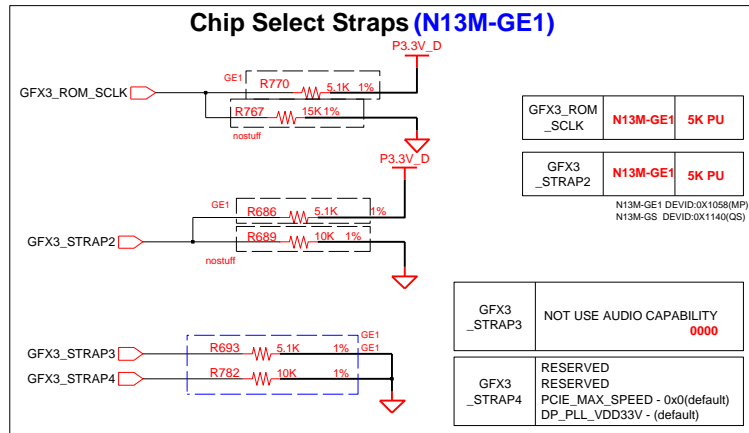
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N13x STRAP

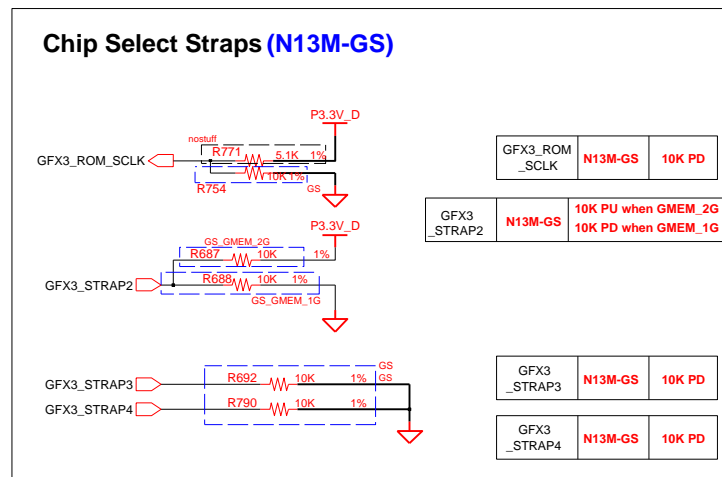
Function Straps



Chip Select Straps (N13M-GE1)



Chip Select Straps (N13M-GS)



N13M-GS

STRAP PIN	STRAP MAPPING	Resistance	Polarity
STRAP0	RAMCFG[0]	10K ohm	Pull-up to 3V3 for binary '1' Pull-down to GND for binary '0'
STRAP1	RAMCFG[1]	10K ohm	
STRAP2	RAMCFG[2]	10K ohm	Samsung 64M x 16 gDDR3 0011
STRAP3	RAMCFG[3]	10K ohm	Samsung 128M x 16 gDDR3 0101
ROM_SO	VGA_DEVICE	10K ohm	Pull-down to GND(no display)
ROM_SI	SUB_VENDOR	10K ohm	Pull-up to 3V3 if VBIOS ROM exists Pull-down to GND if no VBIOROM
ROM_SCLK	SMB_ALT_ADDR	10K ohm	Pull-down to GND
STRAP4	PCI_MAX_SPEED	10K ohm	Pull-down to GND

RESISTOR	PULL UP	PULL DOWN
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

N13M-GE1

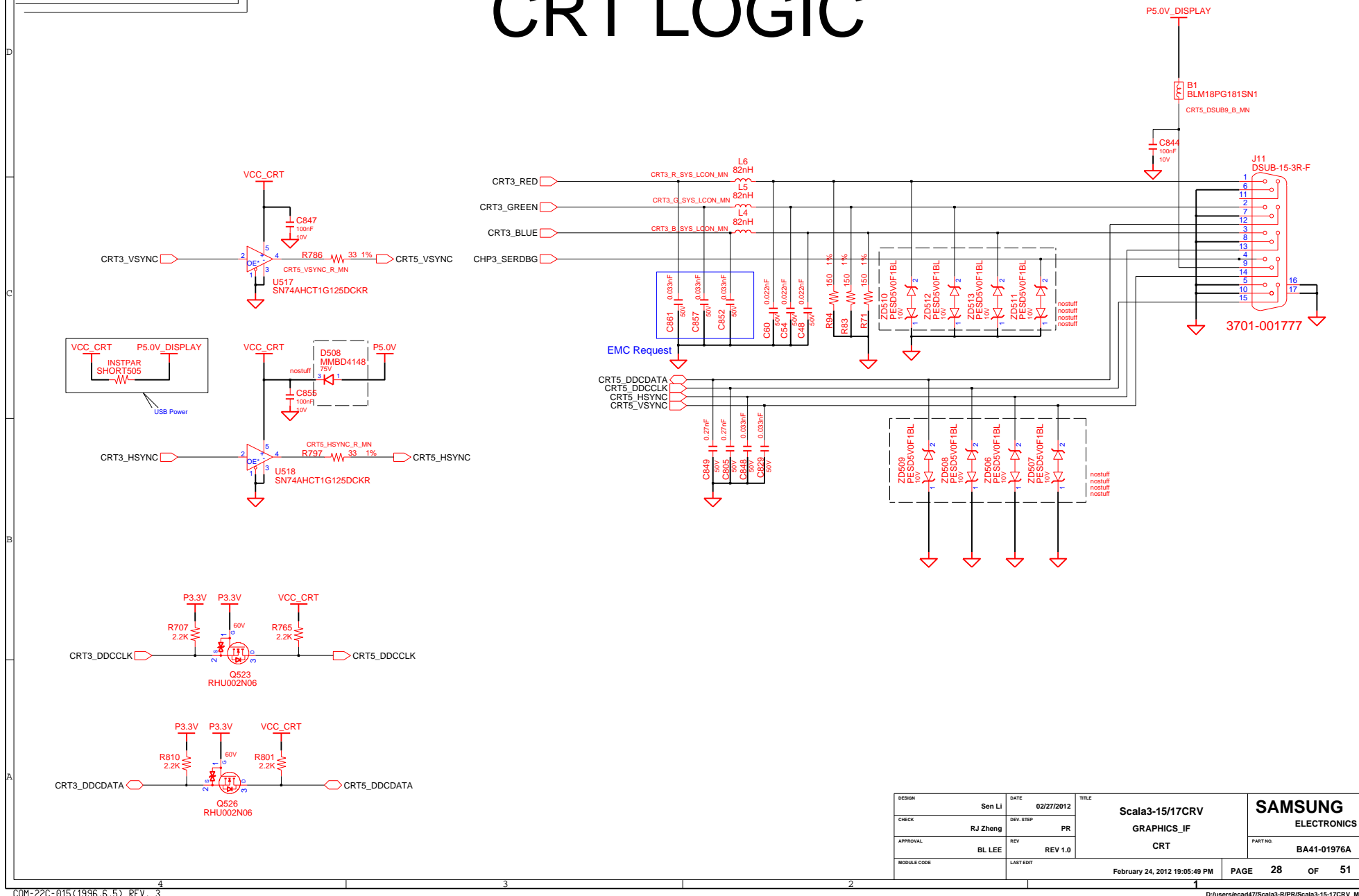
STRAP PIN	BIT 3	BIT 2	BIT 1	BIT0
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
ROM_SO	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
STRAP3	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	RESERVED	RESERVED	PCIE_MAX_SPEED	DP_PLL_VDD33V

DESIGN	Sen Li	DATE	02/27/2012	TITLE	Scala3-15/17CRV	SAMSUNG ELECTRONICS
CHECK	RJ Zheng	DEV. STEP	PR		GRAPHIC Strap	
APPROVAL	BL LEE	REV	REV 1.0		GRAPHIC Strap	
MODULE CODE		LAST EDIT			February 24, 2012 19:05:49 PM	PAGE 26 OF 51

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CRT LOGIC



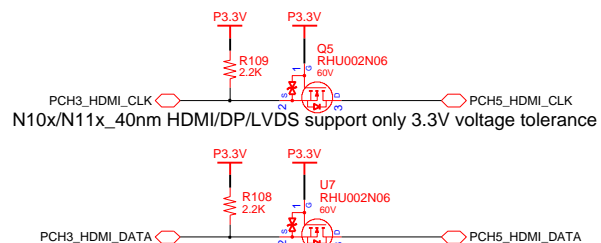
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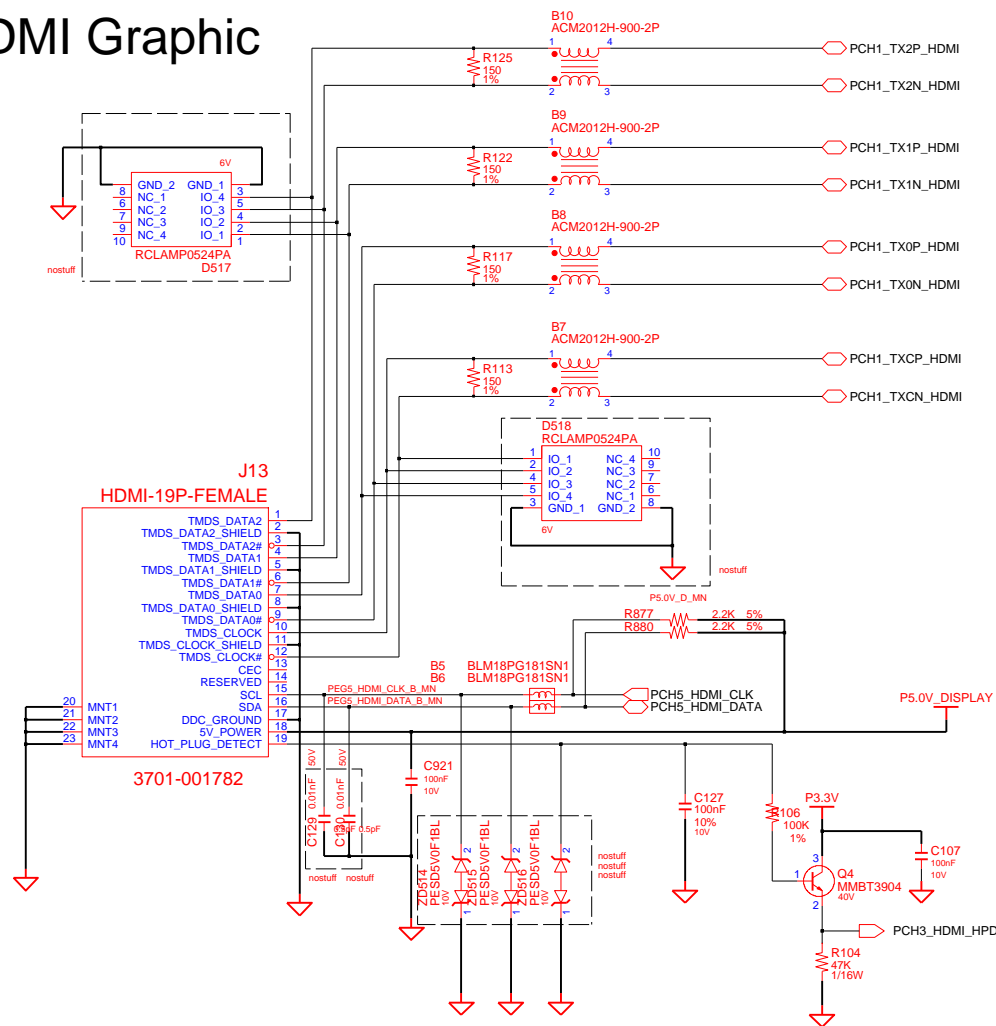
STANDARD NET NAME

Display from PCH	Display from GPU
PCH3_HDMI_xxx	PEG3_HDMI_xxx
PCH1_xxxx_HDMI	PEG3_xxxx_HDMI

FOR HDMI VERIFICATION TEST



HDMI Graphic



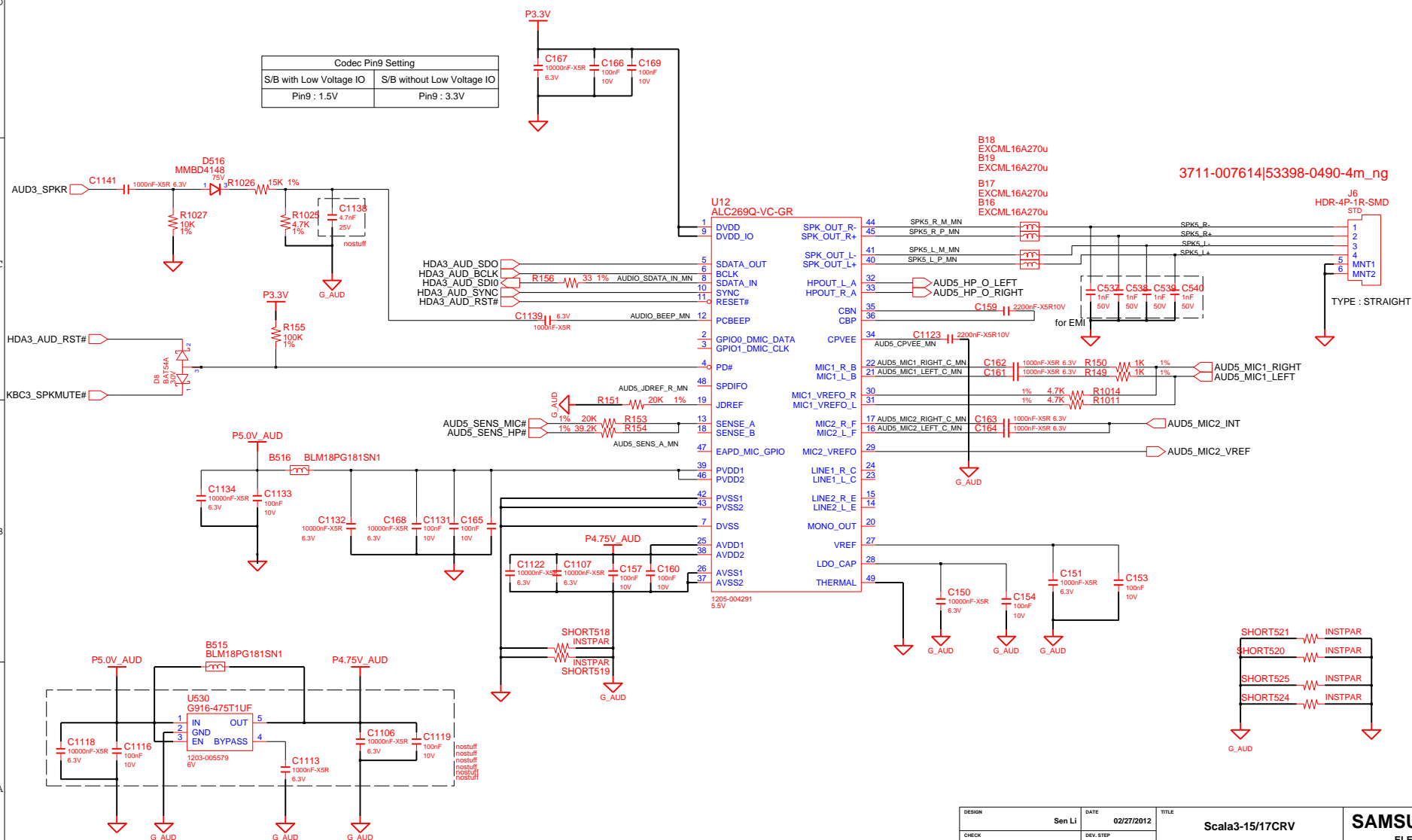
DESIGN	Sen Li	DATE	02/27/2012	TITLE	Scala3-15/17CRV	SAMSUNG ELECTRONICS
CHECK	RJ Zheng	DEV. STEP	PR		GRAPHICS_IF	
APPROVAL	BL LEE	REV	REV 1.0		HDMI	
MODULE CODE		LAST EDIT		February 24, 2012 10:05:49 PM	PAGE 29 OF 51	PART NO. BA41-01976A

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HD AUDIO

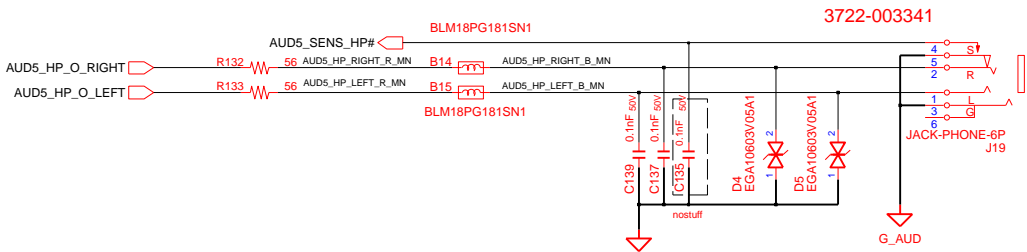
Codec Pin9 Setting	
S/B with Low Voltage IO	S/B without Low Voltage IO
Pin9 : 1.5V	Pin9 : 3.3V



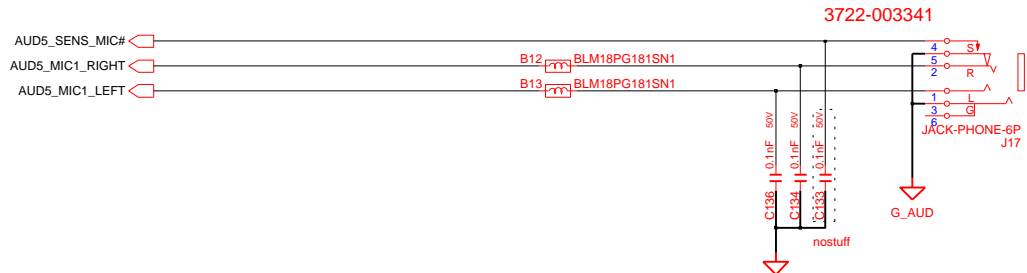
DESIGN	Sen Li	DATE	02/27/2012	TITLE	Scala3-15/17CRV	SAMSUNG ELECTRONICS
CHECK	RJ Zheng	DEV. STEP	PR		HDA_CODEC	
APPROVAL	BL LEE	REV	REV 1.0		AUDIO CODEC ALC269	
MODULE CODE		LAST EDIT				
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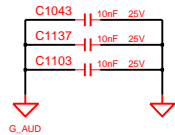
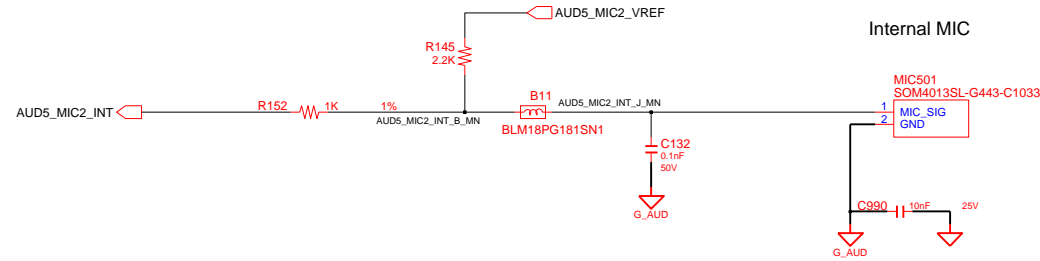
HEADPHONE



MIC JACK



Internal MIC

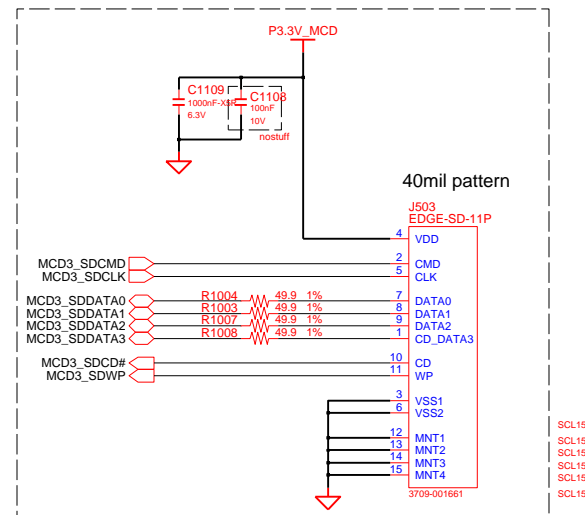
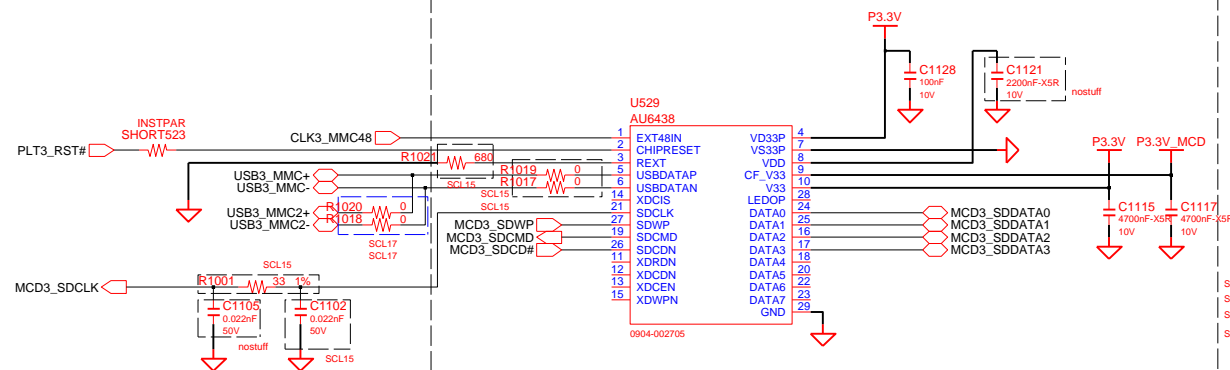


DESIGN	Sen Li	DATE	02/27/2012	TITLE	Scala3-15/17CRV	SAMSUNG ELECTRONICS
CHECK	RJ Zheng	DEV. STEP	PR		HDA_CODEC	
APPROVAL	BL LEE	REV	REV 1.0		AUDIO JACK	
MODULE CODE		LAST EDIT		February 24, 2012 19:05:49 PM	PAGE 31 OF 51	BA41-01976A

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4 IN 1 CARD

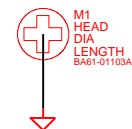
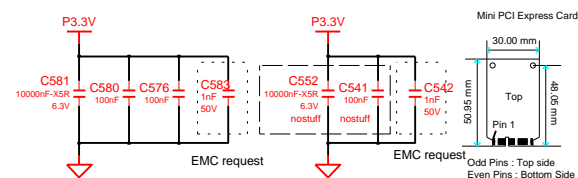
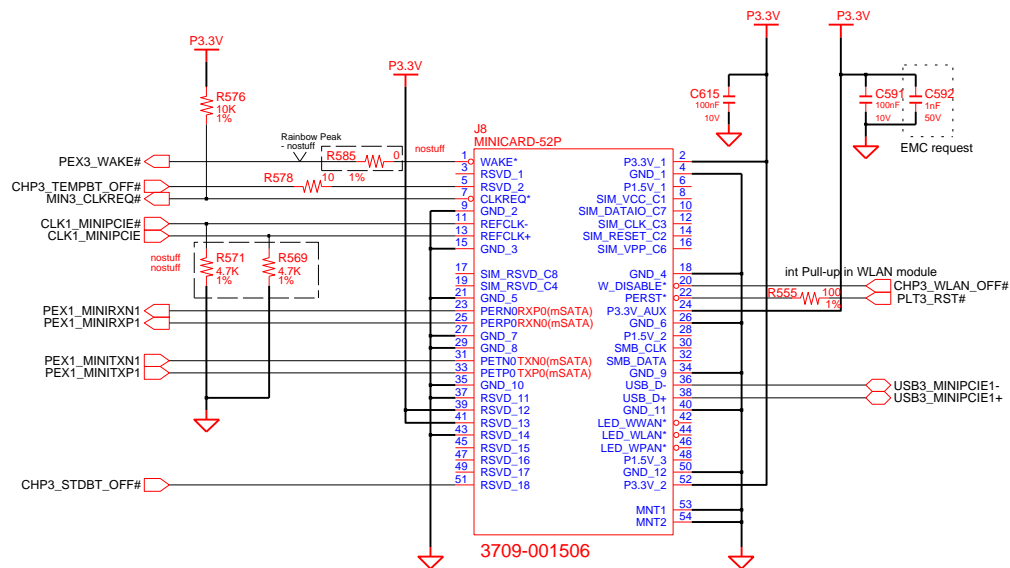


DESIGN	Sen Li	DATE	02/27/2012	TITLE	Scala3-15/17CRV	SAMSUNG ELECTRONICS
CHECK	RJ Zheng	DEV. STEP	PR		MULTICARD	
APPROVAL	BL LEE	REV	REV 1.0		4 IN 1 CARD(AU6438)	
MODULE CODE		LAST EDIT	February 24, 2012 19:05:49 PM	PAGE	33 OF 51	

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WLAN, 7mm

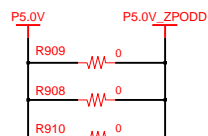
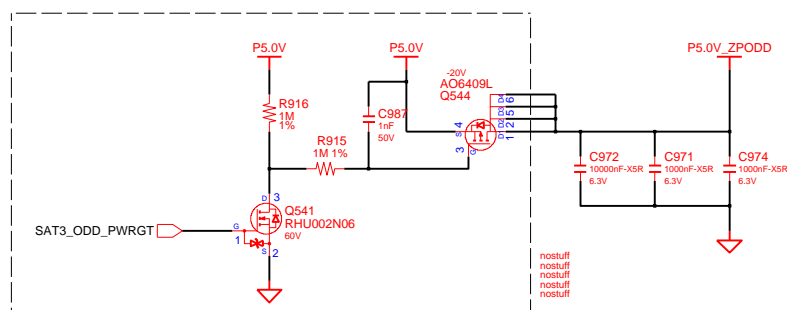


DESIGN	Sen Li	DATE	02/27/2012	TITLE	Scala3-15/17CRV	SAMSUNG ELECTRONICS
CHECK	RJ Zheng	DEV. STEP	PR		MINI_PCIE_CONN	
APPROVAL	BL LEE	REV	REV 1.0		WLAN	
MODULE CODE		LAST EDIT	February 24, 2012 19:05:49 PM	PAGE	34	OF 51

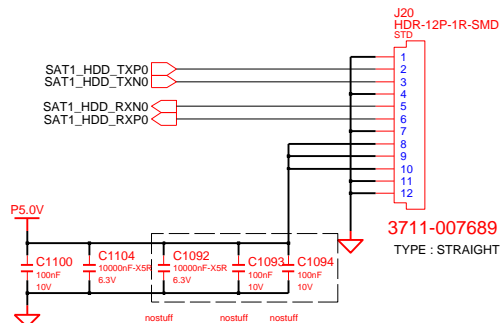
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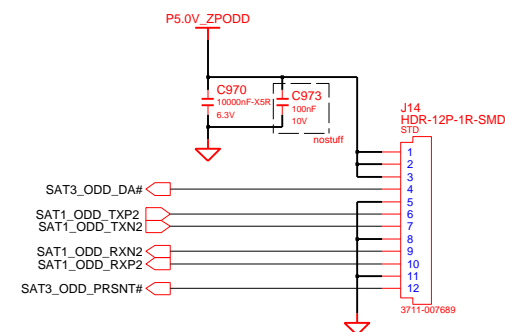
SATA I/F CONN



SATA HDD CONN



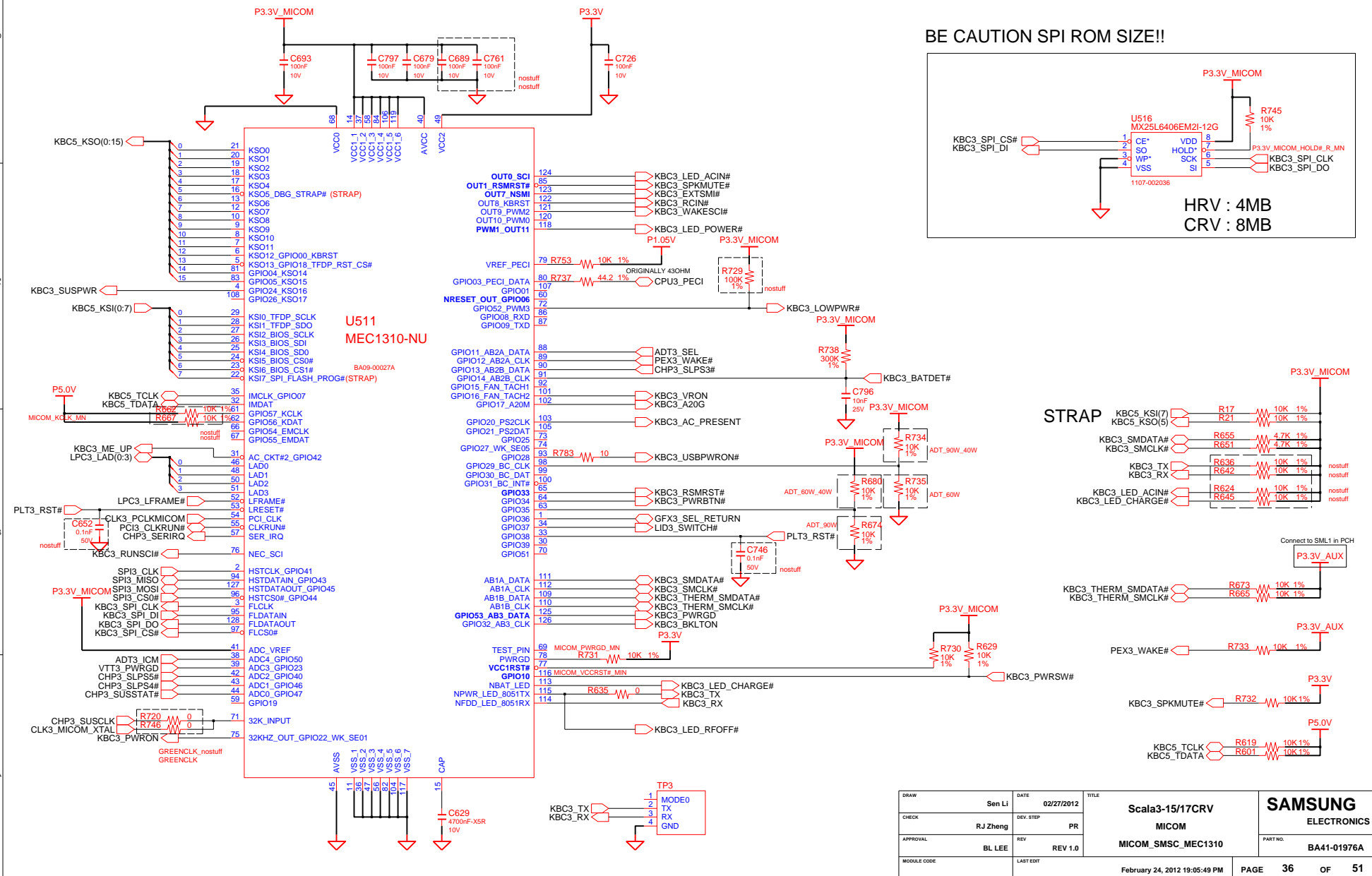
SATA ODD CONN



DESIGN	Sen Li	DATE	02/27/2012	TITLE	Scala3-15/17CRV	SAMSUNG ELECTRONICS
CHECK	RJ Zheng	DEV. STEP	PR		SATA_DEVICES	
APPROVAL	BL LEE	REV	REV 1.0		HDD & ODD SUB CONNECTOR	
MODULE CODE		LAST EDIT		February 24, 2012 19:05:49 PM	PAGE 35 OF 51	PART NO. BA41-01976A

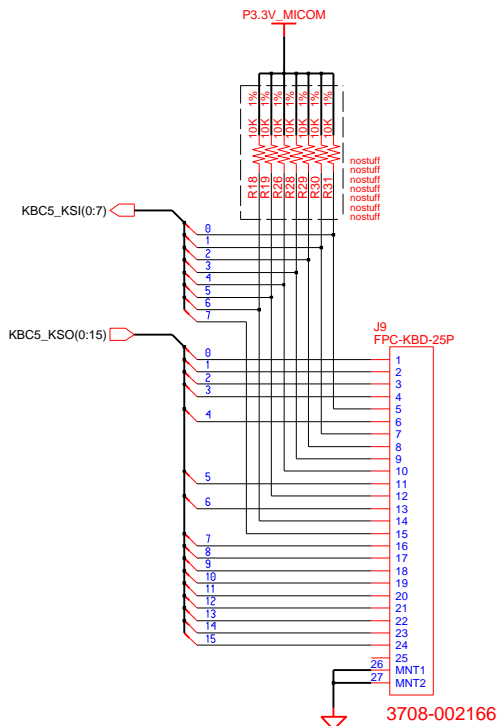
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MAIN BOARD (MICOM)

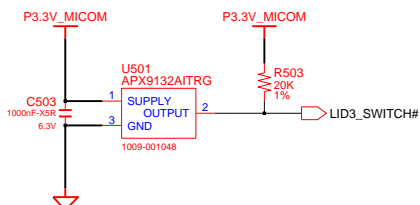


Micom Glue Logic

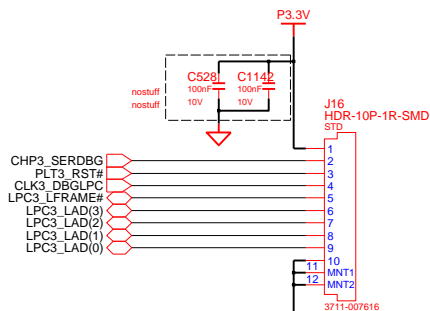
KEYBOARD



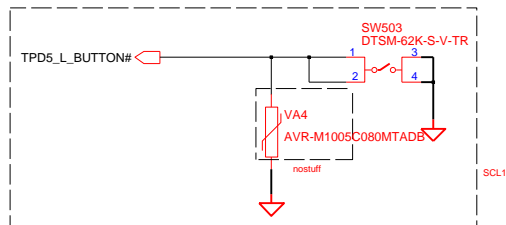
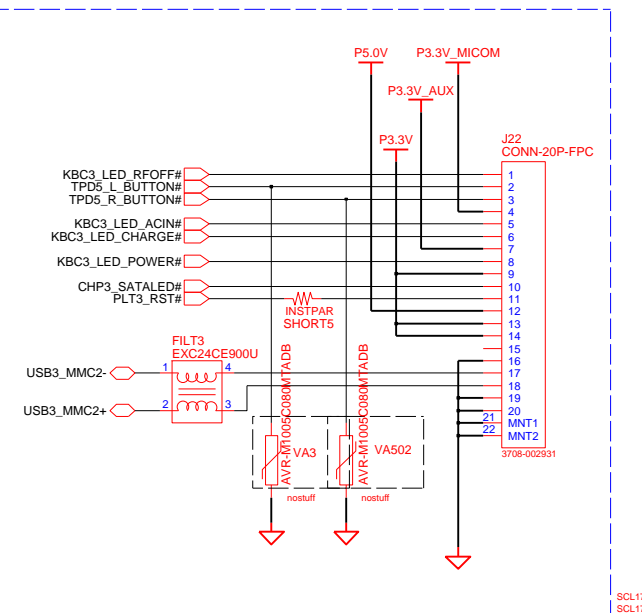
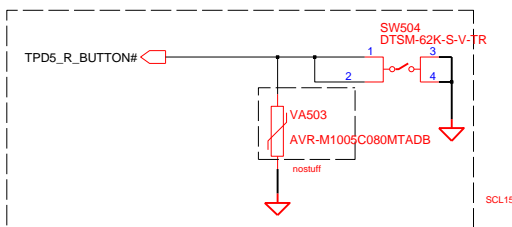
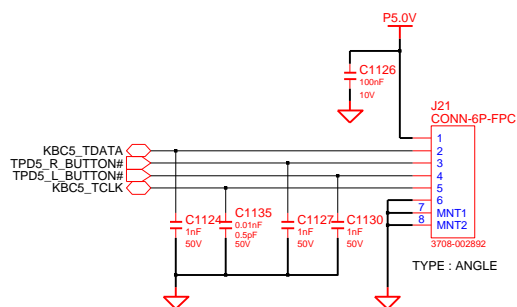
LID_SWITCH



17" 80H PORT DEBUG



TOUCHPAD



DESIGN	Sen Li	DATE	02/27/2012	TITLE	Scala3-15/17CRV	SAMSUNG ELECTRONICS
CHECK	RJ Zheng	DEV. STEP	PR		MICOM GLUE LOGIC	
APPROVAL	BL LEE	REV	REV 1.0		KEYBOARD & TOUCHPAD	
MODULE CODE		LAST EDIT				
				February 24, 2012 19:05:49 PM	PAGE 37 OF 51	BA41-01976A

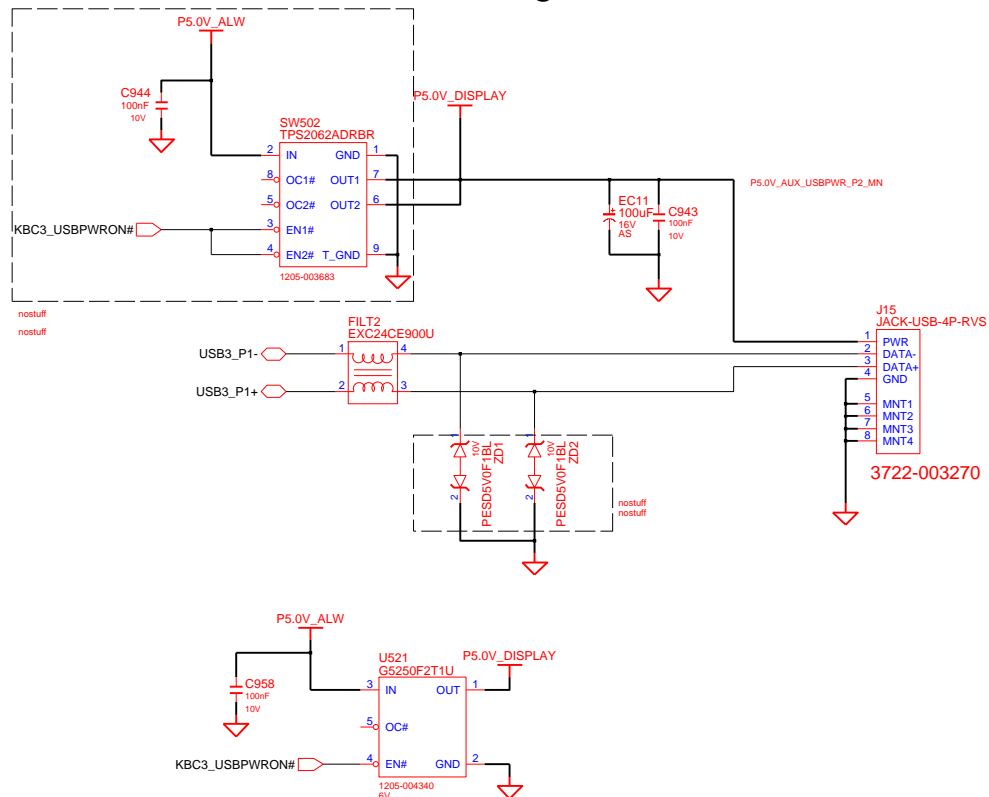
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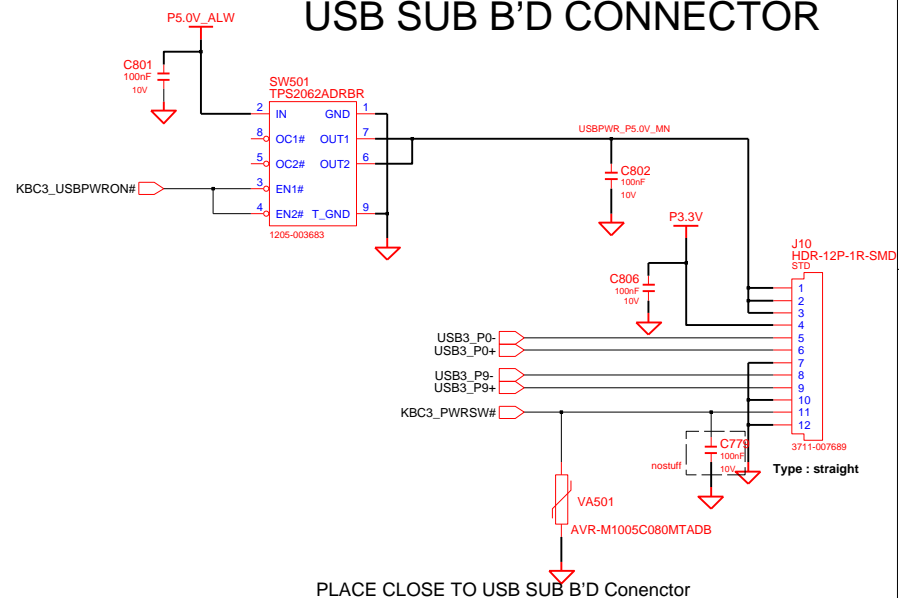
USB Single connector



MAIN TO SUB USB CONN

Right 2USB Port

USB SUB B'D CONNECTOR

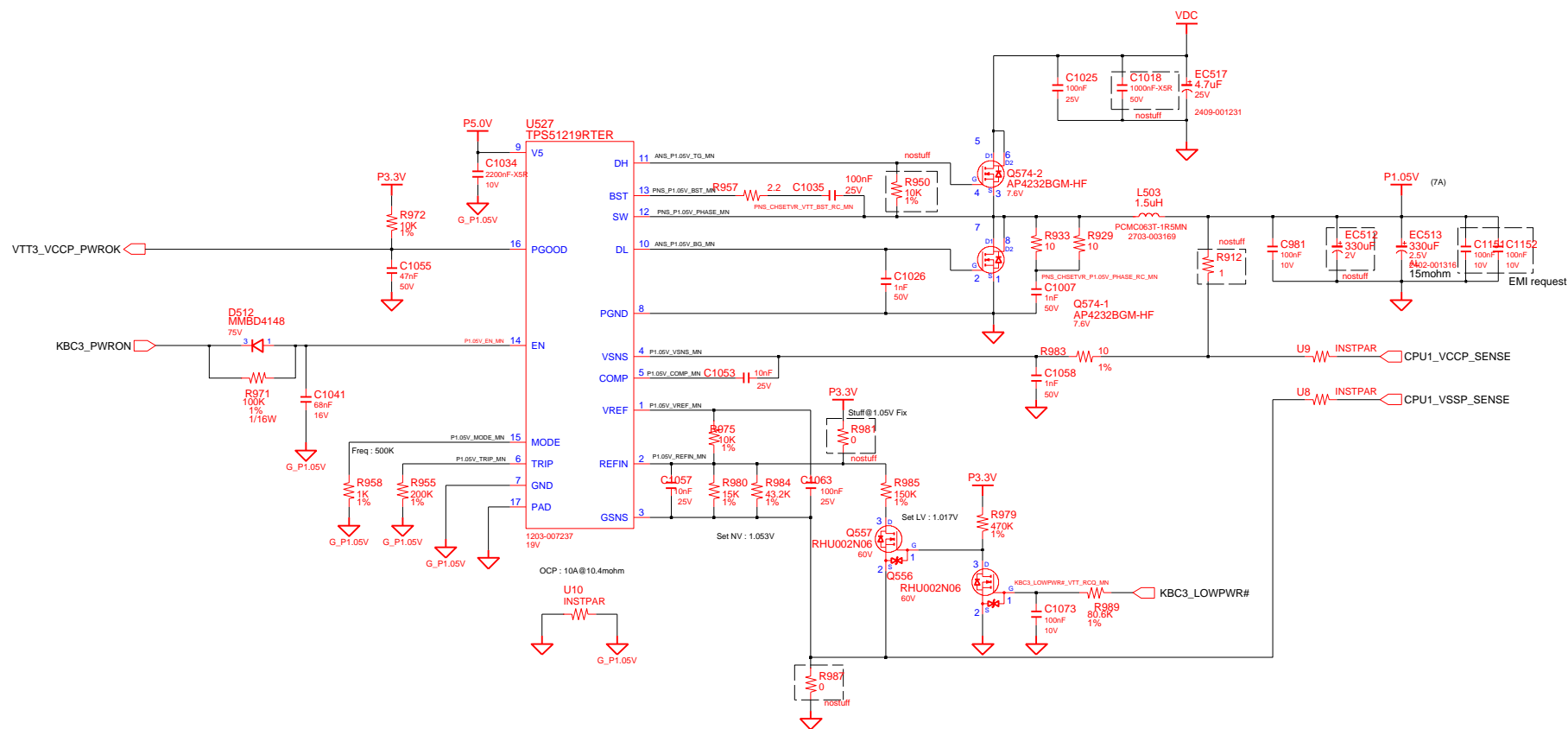


DESIGN	Sen Li	DATE	02/27/2012	TITLE	Scala3-15/17CRV	SAMSUNG ELECTRONICS
CHECK	RJ Zheng	DEV. STEP	PR		USB_CONN	
APPROVAL	BL LEE	REV	REV 1.0		USB Port	
MODULE CODE		LAST EDIT		February 24, 2012 19:05:49 PM	PAGE 39 OF 51	PART NO. BA41-01976A

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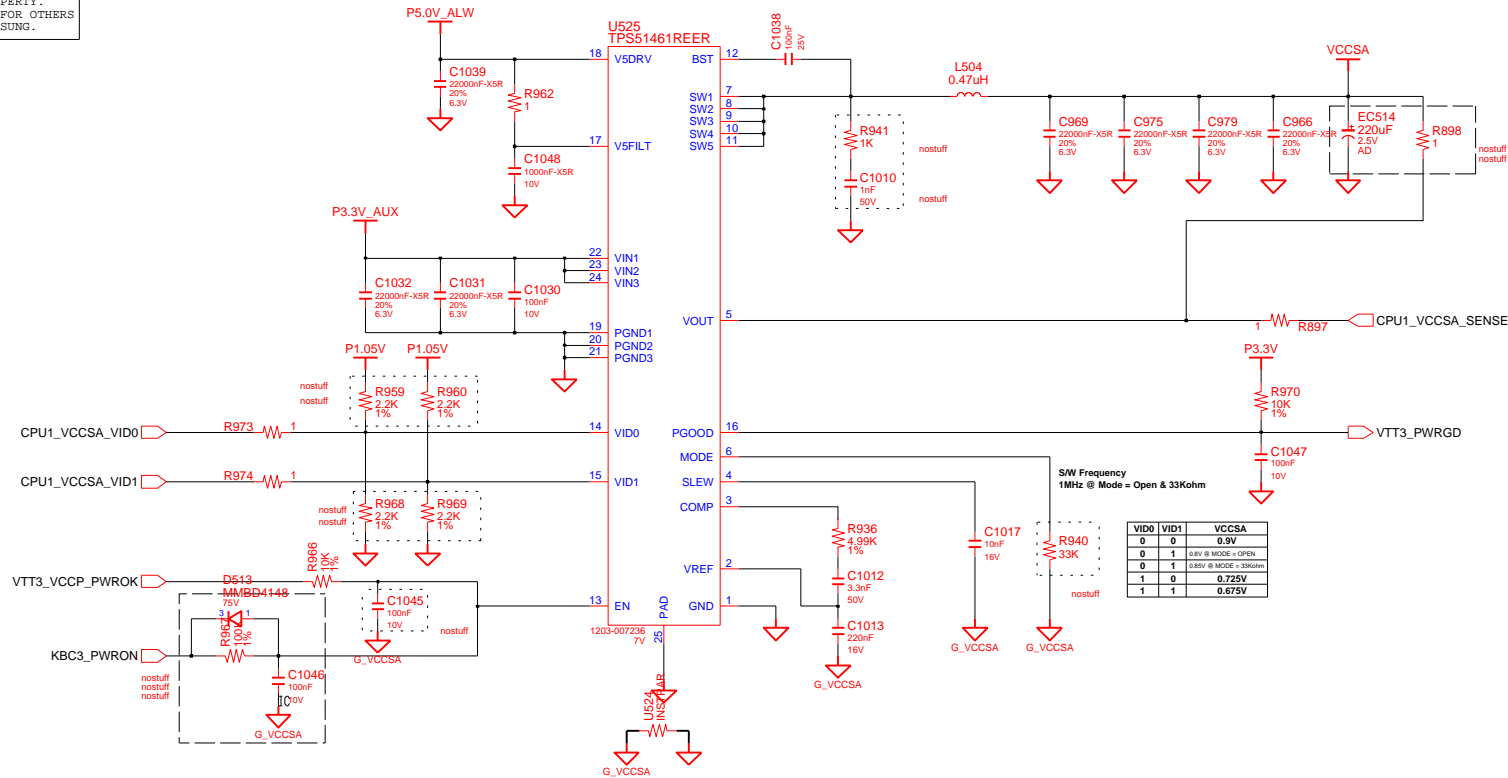
Chipset Power (P1.05V)



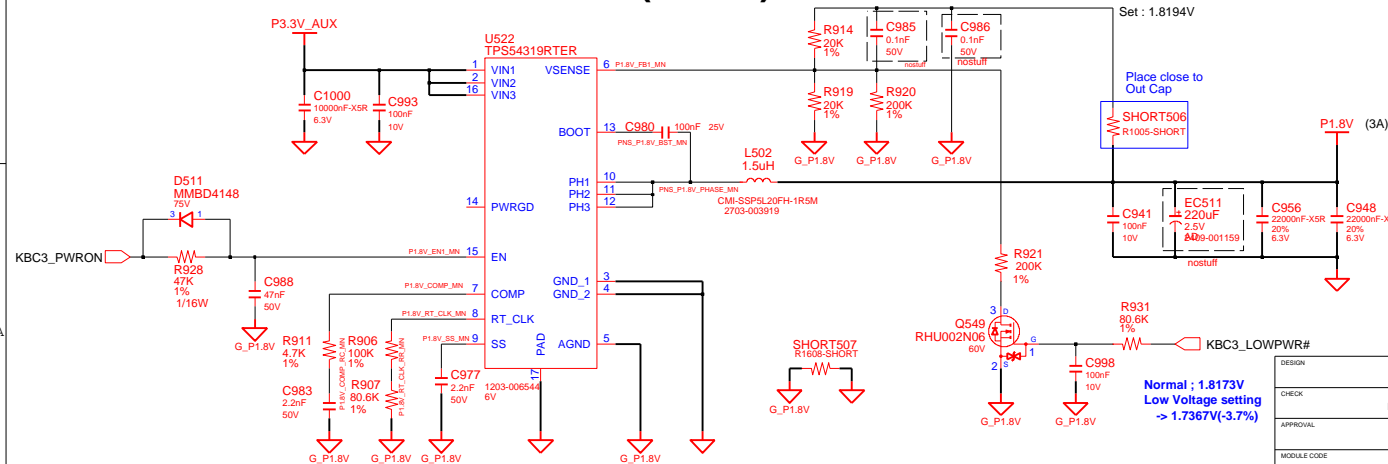
DRAW	Sen Li	DATE	02/27/2012	TITLE	Scale3-15/17CRV	SAMSUNG ELECTRONICS
CHECK	RJ Zheng	DEV. STEP	PR		P1.05V	
APPROVAL	BL LEE	REV	REV 1.0		TI TPS51219	
MODULE CODE	undefined	LAST EDIT	February 24, 2012 19:05:49 PM	PAGE	42	OF 51

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CHIPSET POWER(VCCSA)



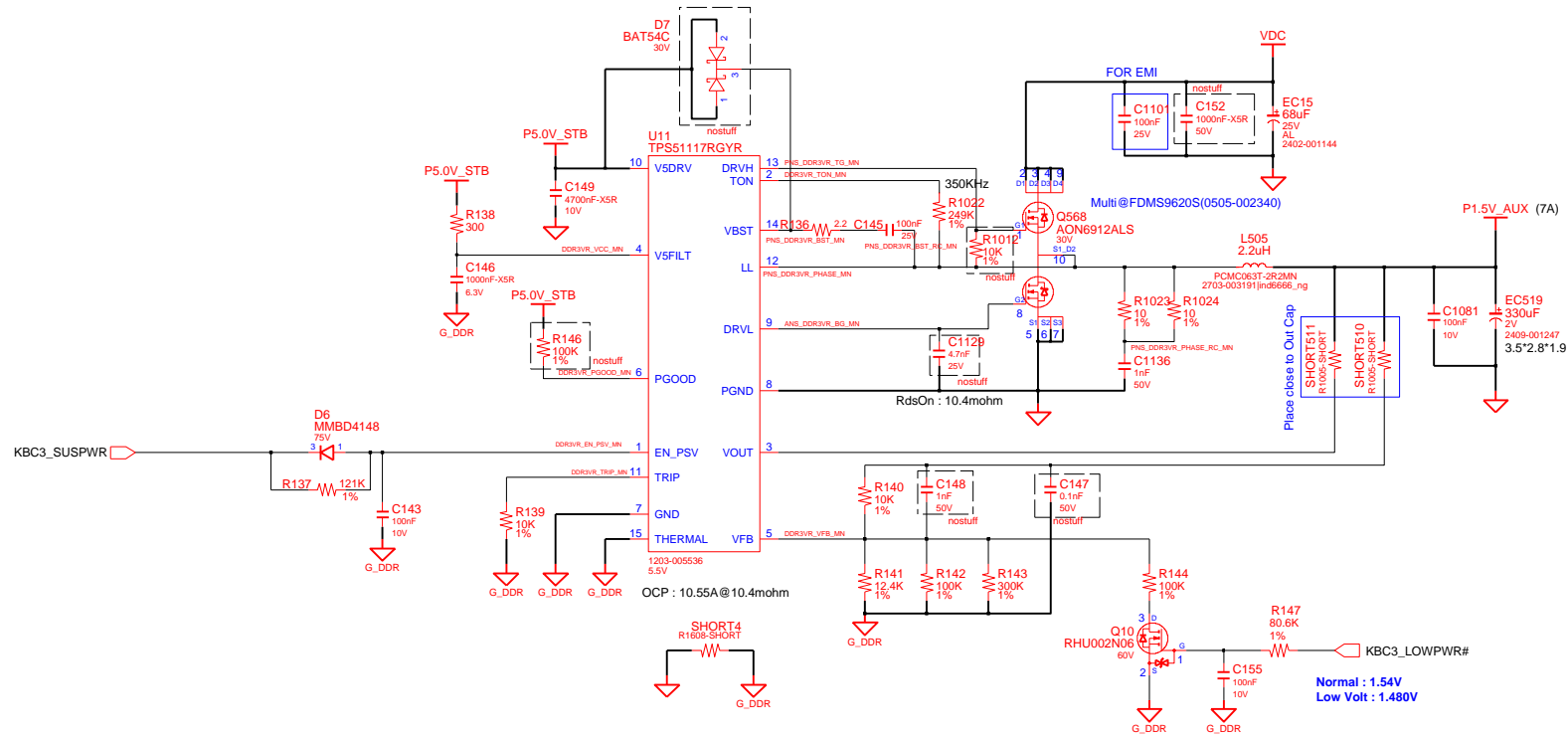
CHIPSET POWER(P1.8V)



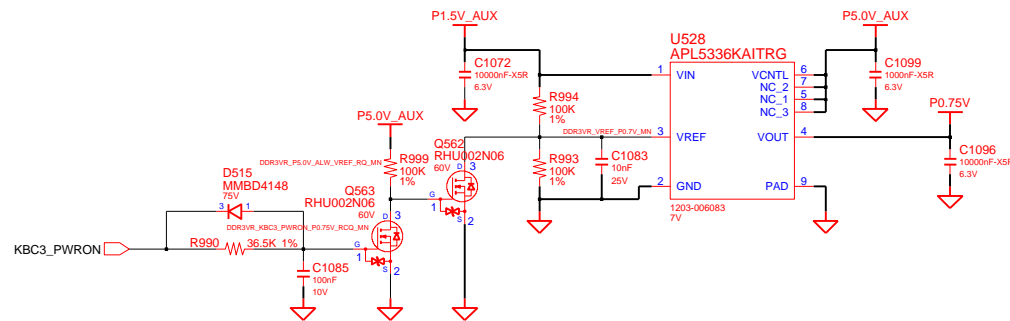
DESIGN	Sen Li	DATE	02/27/2012	TITLE	Scala3-15/17CRV	SAMSUNG ELECTRONICS
CHECK	RJ Zheng	DEV. STEP	PR		VCCSA & P1.8V	
APPROVAL	BL LEE	REV	REV 1.0			PART NO. BA41-01976A
MODULE CODE		LAST EDIT			February 24, 2012 19:05:49 PM	PAGE 43 OF 51

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DDR3 Power



DDR3 VTT(0.75V)



DRAW	Sen Li	DATE	02/27/2012	TITLE	Scala3-15/17CRV	SAMSUNG ELECTRONICS
CHECK	RJ Zheng	DEV. STEP	PR		PWR_MEMORY	
APPROVAL	BL LEE	REV	REV 1.0		DDR3 POWER	
MODULE CODE	undefined	LAST EDIT	February 24, 2012 19:05:49 PM	PAGE	44	OF 51

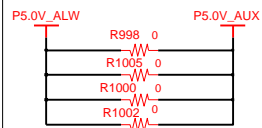
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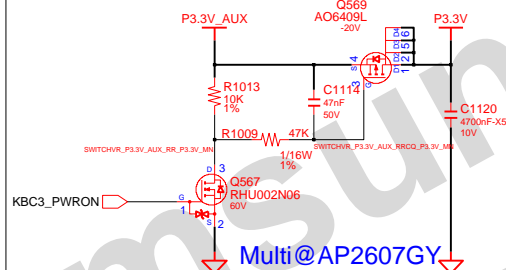
Switched Power 1

(P5.0V -> P3.3V -> EGFX_CORE -> P1.8V -> P1.5V -> P0.75V -> P1.05V -> P0.85V_SA -> CPU_CORE)

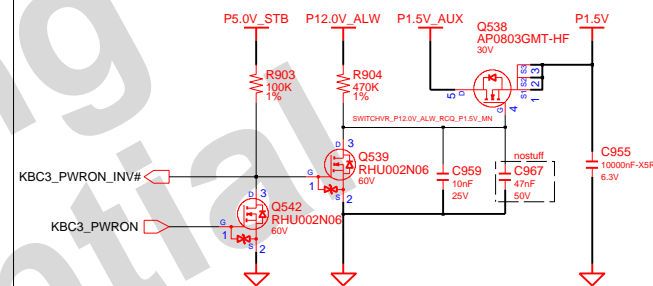
P5.0V_AUX



Switched Power On (P3.3V)

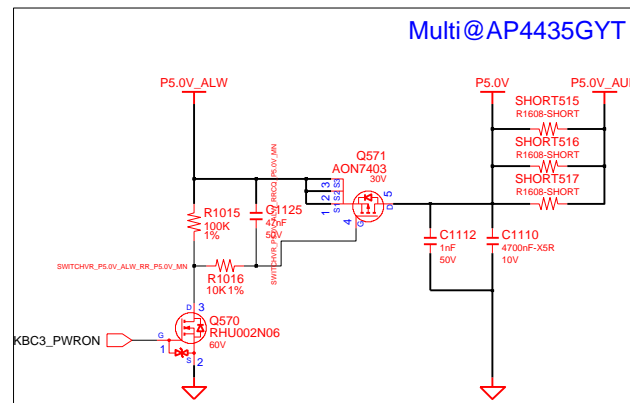


Switched Power On (P1.5V)



For nVIDIA GFX PWR Sequence
NVDD(EGFX_CORE) first and then FBVDDQ(gDDR3)

Switched Power On (P5.0V)



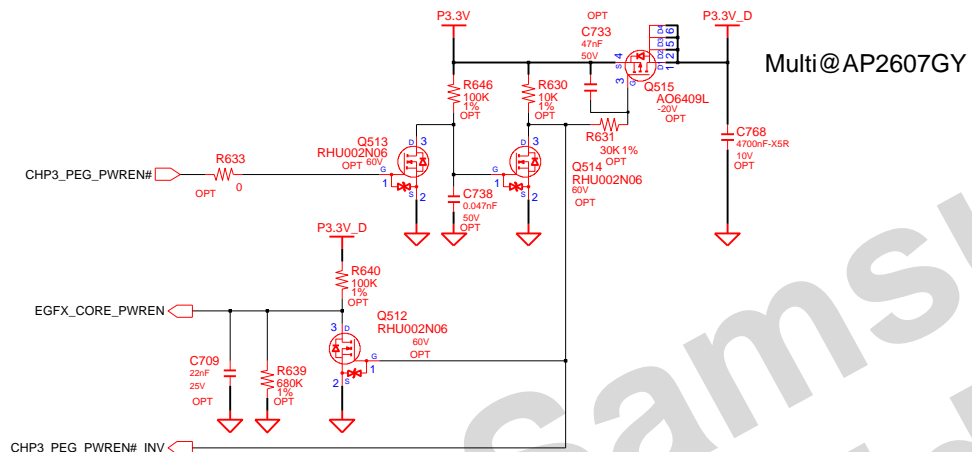
DRAW	Sen Li	DATE	02/27/2012	TITLE	Scala3-15/17CRV	SAMSUNG ELECTRONICS
CHECK	RJ Zheng	DEV. STEP	PR		Switch PWR 1	
APPROVAL	BL LEE	REV	REV 1.0			PART NO. BA41-01976A
MODULE CODE	undefined	LAST EDIT	February 24, 2012 19:05:49 PM	PAGE	47	OF 51

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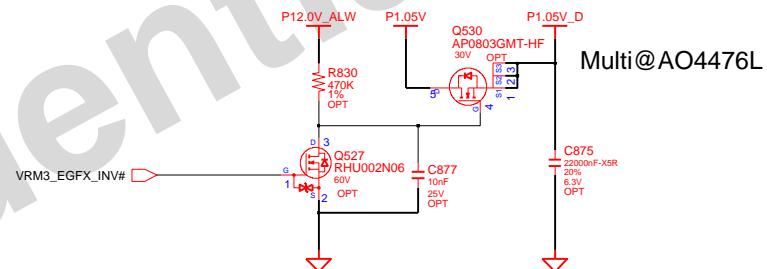
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Switched Power 2 (For nVidia GFX Power Sequence)

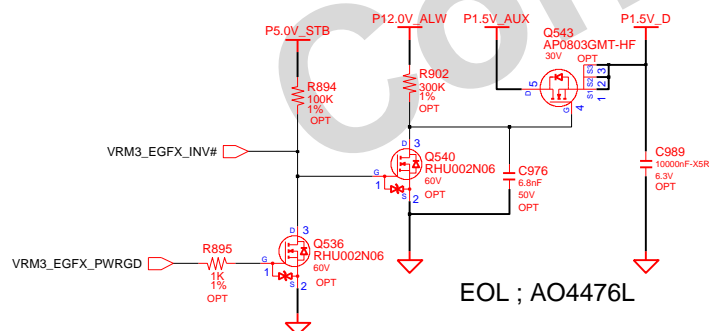
Discrete Switched Power (D3.3V : Max_1.2A)



Discrete Switched Power (D1.05V : Max 3.6A)



Discrete Switched Power (D1.5V : Max 5.0A)

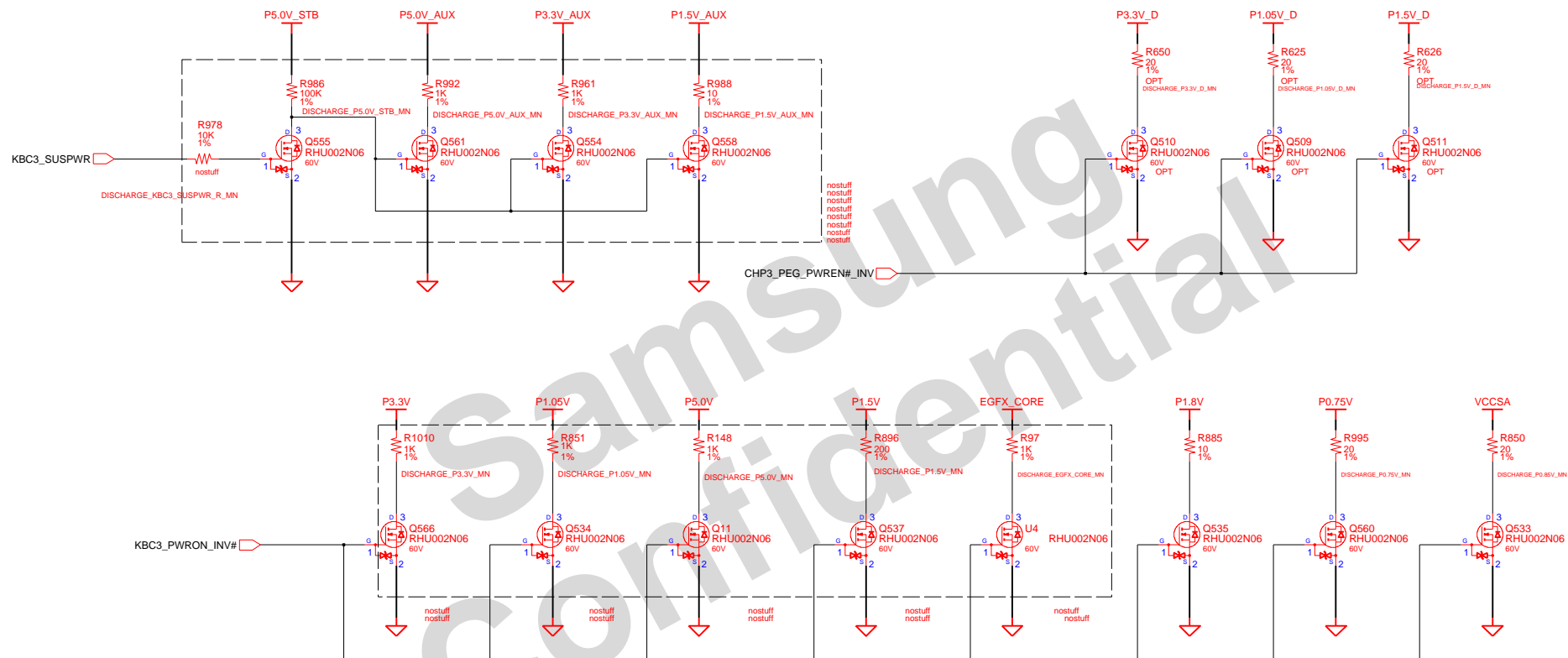


DRAW	Sen Li	DATE	02/27/2012	TITLE	Scala3-15/17CRV	SAMSUNG ELECTRONICS
CHECK	RJ Zheng	DEV. STEP	PR		Switched PWR 2	
APPROVAL	BL LEE	REV	REV 1.0		FOR OPTIMUS PWR	
MODULE CODE		LAST EDIT			February 24, 2012 19:05:49 PM	PART NO. BA41-01976A
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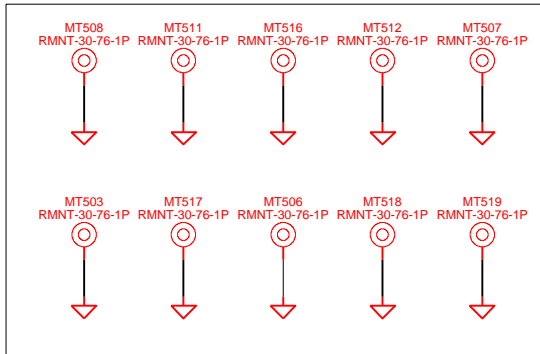
POWER DISCHARGER



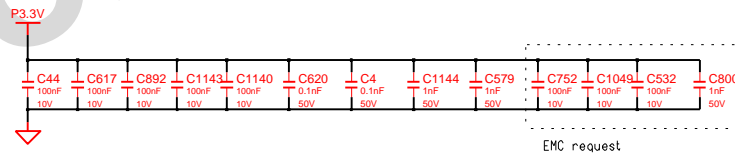
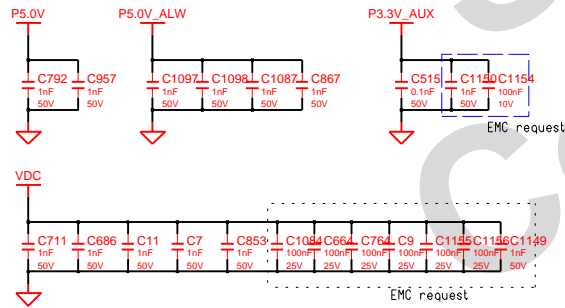
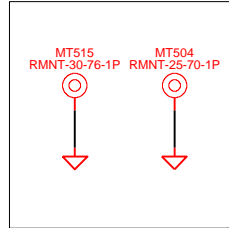
DESIGN	Sen Li	DATE	02/27/2012	TITLE	Scala3-15/17CRV	SAMSUNG ELECTRONICS
CHECK	RJ Zheng	DEV. STEP	PR		PWR_MV_DISCHARGER	
APPROVAL	BL LEE	REV	REV 1.0		DISCHARGING LOGIC	
MODULE CODE		LAST EDIT	February 24, 2012 19:05:49 PM	PAGE	49	OF 51

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Mainboard Mount ((30-76)X8EA)



PCB FIX



DESIGN	Sen Li	DATE	02/27/2012	TITLE	Scala3-15/17CRV	SAMSUNG ELECTRONICS
CHECK	RJ Zheng	DEV. STEP	PR		Mount Hole	
APPROVAL	BL LEE	REV	REV 1.0		Thermal Hole	
MODULE CODE		LAST EDIT	February 24, 2012 19:05:49 PM	PAGE	50	OF 51

